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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Joseph E. Geusic et al.

Title: INTEGRATED CIRCUITS USING OPTICAL WAVEGUIDE INTERCONNECTS FORMED THROUGH A SEMICONDUCTOR WAFER AND METHODS FOR FORMING SAME

Attorney Docket No.: 303.382US2

PATENT APPLICATION TRANSMITTAL

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X **DIVISIONAL** of prior Patent Application No. 09/031,961 (under 37 CFR § 1.53(b)) comprising:
- X Specification (21 pgs, including claims numbered 1 through 44 and a 1 page Abstract).
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TOTAL CLAIMS	17 - 20 =	0	x 18 =	$0.00
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Joseph E. Geusic et al.	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.382US2
Title:	INTEGRATED CIRCUITS USING OPTICAL WAVEGUIDE INTERCONNECTS FORMED THROUGH A SEMICONDUCTOR WAFER AND METHODS FOR FORMING SAME	

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Before taking up the above identified application for Examination, please enter the following amendment.

IN THE SPECIFICATION

In the first line after the title, please insert the following --This application is a divisional of U.S. application, Serial No. 09/031,961, filed on February 26, 1998.--

IN THE CLAIMS

Please cancel claims 1-29 and 31-44. Claim 14-30 remains pending in the application.

CONCLUSION

Applicant will file additional claims in a Supplemental Preliminary Amendment. If the Examiner begins the examination without receiving the new claims, it is respectfully requested that the Examiner contact the below-signed attorney to receive a copy of the new claims.

Respectfully submitted,

JOSEPH E. GEUSIC ET AL.

By their Representatives,

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Integrated Circuits Using Optical Waveguide Interconnects Formed Through a Semiconductor Wafer and Methods for Forming Same

Technical Field of the Invention

The present invention relates generally to the field of integrated circuits and, in particular, to integrated circuits using optical Waveguide interconnects formed through a semiconductor wafer and methods for forming same.

Background of the Invention

Electrical systems typically use a number of integrated circuits that are mounted on a printed circuit board. The individual integrated circuits of the system are typically fabricated on different wafers. Each wafer is tested and separated into individual dies or chips. Individual chips are then packaged as individual integrated circuits. Each integrated circuit includes a number of leads that extend from the packaging of the circuit. The leads of the various integrated circuits, are interconnected to allow information and control signals to be passed between the integrated circuits such that the system performs a desired function. For example, a personal computer includes a wide variety of integrated circuits, e.g., a microprocessor and memory chips, that are interconnected on one or more printed circuit boards in the computer.

While printed circuit boards are useful for bringing together separately fabricated and assembled integrated circuits, the use of printed circuit boards creates some problems which are not so easily overcome. For example, printed circuit boards consume a large amount of physical space compared to the circuitry of the integrated circuits which are mounted to them. It is desirable to reduce the amount of physical space required by such printed circuit boards. Further, assuring the electrical integrity of interconnections between integrated circuits mounted on a printed circuit board is a challenge. Moreover, in certain applications, it is desirable to reduce the physical length of electrical interconnections between devices because of concerns with signal loss or dissipation and interference with and by other integrated circuitry devices.

A continuing challenge in the semiconductor industry is to find new, innovative, and efficient ways of forming electrical connections with and between circuit devices which are fabricated on the same and on different wafers or dies. Relatedly, continuing challenges are posed to find and/or improve upon the packaging techniques utilized to package integrated circuitry devices. As device dimensions continue to shrink, these challenges become even more important.

For reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for an improved technique for interconnecting individual integrated circuits in an electronic system.

Summary of the Invention

The above mentioned problems with integrated circuits and other problems are addressed by the present invention and will be understood by reading and studying the following specification. Integrated circuits are described which use optical waveguides that extend through the thickness of a semiconductor substrate or wafer so as to allow communication between integrated circuits formed on opposite sides of a single wafer, on opposite sides of two wafers that are bonded together, formed on wafers in a stack that are bonded together, or other appropriate configuration of wafers.

In particular, in one embodiment, a method for interconnecting first and second integrated circuits is provided. The first integrated circuit is formed on a working surface of a first semiconductor substrate. At least one high aspect ratio hole is formed through the first semiconductor substrate. The high aspect ratio hole is lined with a material having a high reflectivity for light to form an optical waveguide. The first integrated circuit is coupled to the second integrated circuit through the optical waveguide. In one embodiment, the second integrated circuit is formed on a second surface of the first semiconductor substrate, opposite the working surface of the first semiconductor substrate. In another embodiment, the second integrated circuit is formed on a working surface of a second semiconductor substrate. The second

semiconductor substrate is bonded to the first semiconductor substrate such that the first and second integrated circuits are coupled together through the optical waveguide in the first semiconductor substrate. In another embodiment, the surfaces of the first and second semiconductor substrates that are bonded together are located on sides of the first and second semiconductor substrates that are opposite the working surfaces of the first and second semiconductor substrates, respectively.

In another embodiment, an electronic system is provided. The electronic system includes at least one semiconductor wafer. The electronic system includes a number of integrated circuits. At least one integrated circuit is formed on the at least one semiconductor wafer. The at least one semiconductor wafer includes at least one optical waveguide formed in a high aspect ratio hole that extends through the thickness of the at least one semiconductor wafer. Further, at least one optical transmitter and at least one optical receiver are associated with the at least one optical waveguide. The optical transmitter and optical receiver transmit optical signals between selected integrated circuits of the electronic system.

In another embodiment, an integrated circuit is provided. The integrated circuit includes a functional circuit formed on a wafer. A number of optical waveguides are formed in high aspect ratio holes that extend through the wafer. The optical waveguides include a highly reflective material that is deposited so as to line an inner surface of the high aspect ratio holes.

In another embodiment, a method for forming an integrated circuit in a semiconductor wafer with an optical waveguide that extends through the semiconductor wafer is provided. A functional circuit is formed in a first surface of a semiconductor wafer. A number of etch pits are formed in the first surface of the semiconductor wafer at selected locations in the functional circuit. An anodic etch of the semiconductor wafer is performed such that high aspect ratio holes are formed through the semiconductor wafer from the first surface to a second, opposite surface. A highly reflective layer of material is formed on an inner surface of the high aspect ratio holes such that the holes have an opening extending through the semiconductor wafer with a

diameter that is at least three times the cut-off diameter. The optical fiber is selectively coupled to the functional circuit.

In another embodiment, a method for forming an optical waveguide through a semiconductor substrate is provided. The method includes forming at least one high aspect ratio hole through the semiconductor substrate that passes through the semiconductor substrate from a first working surface to a surface opposite the first working surface. Further, the high aspect ratio hole is lined with a material having a high reflectivity for light. In one embodiment, the at least one high aspect ratio hole is etched in the semiconductor substrate using an anodic etch. In one embodiment, etch pits are formed in the working surface of the semiconductor substrate prior to the anodic etch such that the at least one high aspect ratio hole is formed at the location of the etch pits. In one embodiment, the high aspect ratio holes are lined with a layer of tungsten and a layer of aluminum. In one embodiment, the tungsten layer is formed using a silicon reduction process and a silane reduction process. In one embodiment, the high aspect ratio hole is lined with a layer of aluminum material. In one embodiment, the layer of aluminum material has a thickness of approximately 300 angstroms. In one embodiment, the optical waveguide includes an opening extending through the semiconductor substrate with a cross-sectional diameter of at least three times the cut-off diameter.

Brief Description of the Drawings

Figures 1A, 1B, and 1C are elevational views of exemplary embodiments of integrated circuits that use a semiconductor wafer having an optical waveguide formed in an high aspect ratio hole that extends through the semiconductor wafer according to the teachings of the present invention.

Figure 2, 3, 4, 5, and 6 are views of a semiconductor wafer at various points of an illustrative embodiment of a method for forming an optical waveguide through the wafer according to the teachings of the present invention.

Detailed Description

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific illustrative embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

In the following description, the terms wafer and substrate are interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a supporting semiconductor or insulating material, combinations of such layers, as well as other such structures that are known in the art.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizonal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

Figure 1A is an elevational view of an embodiment of the present invention. Electronic system 105a includes semiconductor wafer 100a. Semiconductor wafer 100a includes at least one optical waveguide 102a that provides a path for transmitting signals between functional circuit 108a on a first working surface of semiconductor wafer 100a and functional circuit 109a on a second, opposite working surface of semiconductor wafer 100a. It is noted that a number of optical waveguides can be

formed through semiconductor wafer 100a. The single optical waveguide 102a is shown by way of example and not by way of limitation.

Optical waveguide 102a is formed in a high aspect ratio hole in semiconductor wafer 100a. The high aspect ratio hole is formed using, for example, an anodic etching technique as described in more detail below. Typically, the high aspect ratio holes have an aspect ratio in the range of approximately 100 to 200. Conventionally, a semiconductor wafer has a thickness in the range of approximately 100 to 1000 microns. Thus, the high aspect ratio holes used to form the optical waveguides can be fabricated with a diameter that is in the range from approximately 0.5 microns to approximately 10 microns.

Optical waveguide 102a is coupled to functional circuits 108a and 109a. For example, optical transmitter 104a is coupled to one end of optical waveguide 102a and optical receiver 106a is coupled to a second, opposite end of optical waveguide 102a. Optical transmitter 104a is also coupled to a node of functional circuit 108a and optical receiver 106a is coupled to a node of functional circuit 109a. In one embodiment, optical transmitter 104a comprises a gallium arsenide transmitter that is bonded to a surface of semiconductor wafer 100a using conventional wafer bonding techniques. In this embodiment, optical receiver 106a comprises a silicon photodiode detector formed in a surface of semiconductor wafer 100a. In other embodiments, other appropriate optical receivers and transmitters may be used to transmit signals over optical waveguide 102a.

Optical waveguides 102a include reflective layer 110a and hollow core 112a. Reflective layer 110a comprises a highly reflective material such as aluminum or other material that can be used to line the high aspect ratio hole with a mirror-like surface. When aluminum is used, a thickness of approximately 300 angstroms effectively achieves full reflectivity.

Reflective layer 110a serves to contain optical waves within optical waveguide 102a. This is desirable for at least two reasons. First, this reduces loss of the optical signal into the surrounding semiconductor material of wafer 100a. Second, this also

reduces photogeneration of carriers in the surrounding semiconductor material of wafer 100a that might interfere with normal operation of other integrated circuitry in electrical system 105a.

Optical waveguide 102a should have sufficient diameter to be above cut-off for transmission of light waves. Equation (1) can be used to determine the cut-off diameter, D_0, for transmission of optical waves in the optical waveguide. Optical waveguide 102a should have a diameter that is at least three times the cut-off diameter. In some cases, a diameter that is ten times the cut-off diameter can be used.

$$D_0 = 0.59 \frac{\lambda_0}{n} \quad (1)$$

The term λ_0 is the free-space wavelength and n is the index of refraction for the material within the optical guide. For a case where λ_0 is 1 micron and n is 1 (e.g., air in the center of the waveguide), a 6 micron diameter for optical waveguide 102 is reasonable.

It is noted that optical waveguide 102a could be filled with a material with an index of refraction that is greater than 1. However, the material used for reflective layer 110, e.g., aluminum, would have to survive the deposition of the material.

Optical waveguides can be added to circuits using a conventional layout for the circuit without adversely affecting the surface area requirements of the circuit. Conventional circuits typically include pads formed on the top surface of the semiconductor wafer that are used to connect to leads of the integrated circuit through bonding wires. Advantageously, the bonding wires of conventional circuits can be replaced by optical waveguides 102a to allow signals to be passed between various integrated circuits of electrical system 105a without the need to attach the individual integrated circuits to a printed circuit board. This allows a substantial space savings in the design of electrical systems along with overcoming concerns related to signal loss or

dissipation and interference with and by other integrated circuitry devices in the electrical system.

Figures 1B and 1C show additional embodiments of electronic systems using optical waveguides formed through integrated circuits to interconnect various integrated circuits. In the embodiment of Figure 1B, integrated circuits 108b and 109b are formed in working surfaces of semiconductor wafers 100b and 101b. Surfaces opposite the working surfaces of semiconductor wafers 100b and 101b are bonded together using conventional wafer bonding techniques. Optical waveguide 102b transmits signals between integrated circuits 108b and 109b. A portion of optical waveguide 102b is formed in each of the semiconductor wafers 100b and 101b. In the embodiment of Figure 1C, semiconductor wafers 100c and 101c are stacked with the working surface of semiconductor wafer 101c beneath the surface of semiconductor wafer 100c that is opposite the working surface of semiconductor wafer 100c. In this embodiment, optical waveguide 102c is formed within semiconductor wafer 100c.

Figure 2, 3, 4, 5, and 6 are views of semiconductor wafer 200 at various points of an illustrative embodiment of a method for forming optical waveguides through a semiconductor wafer according to the teachings of the present invention. Functional circuit 202 is formed in an active region of semiconductor wafer 200. For purposes of clarity, the Figures only show the formation of two optical waveguides through semiconductor wafer 200. However, it is understood that with a particular functional circuit any appropriate number of optical waveguides can be formed. Essentially, the optical waveguides are formed in the same space on the surface of semiconductor wafer 200 that is conventionally used to form bonding pads for leads. In a conventional circuit, the leads of the integrated circuit are connected to a printed circuit board which routes signals to other integrated circuits. The optical waveguides advantageously remove the need for a printed circuit board to interconnect the functional circuits formed on individual semiconductor wafers.

As shown in Figure 2, photo resist layer 204 is formed on surface 206 of semiconductor substrate 200. Photo resist layer 204 is patterned to provide openings

208 at points on surface 206 where high aspect ratio holes are to be formed through semiconductor wafer 200.

As shown in Figure 3, etch pits 210 are formed by standard alkaline etching through openings 208 in photo resist layer 204. Photo resist layer 204 is then removed.

Figure 4 is a schematic diagram that illustrates an embodiment of a layout of equipment used to carry out an anodic etch that is used to form high aspect ratio holes 250 of Figure 5. Typically, holes 250 have an aspect ratio in the range of 100 to 200. Bottom surface 262 of semiconductor wafer 200 is coupled to voltage source 234 by positive electrode 230. Further, negative electrode 232 is coupled to voltage source 234 and is placed in a bath of 6% aqueous solution of hydrofluoric acid (HF) on surface 206 of semiconductor wafer 200.

In this example, illumination equipment 236 is also included because semiconductor wafer 200 is n-type semiconductor material. When p-type semiconductor material is used, the illumination equipment is not required. Illumination equipment 236 assures that there is a sufficient concentration of holes in semiconductor wafer 200 as required by the anodic etching process. Illumination equipment 236 includes lamp 238, IR filter 240, and lens 242. Illumination equipment 236 focuses light on surface 262 of semiconductor wafer 200.

In operation, the anodic etch etches high aspect ratio holes through semiconductor wafer 200 at the location of etch pits 210. Voltage source 234 is turned on and provides a voltage across positive and negative electrodes 230 and 232. Etching current flows from surface 206 to positive electrode 230. This current forms the high aspect ratio holes through semiconductor wafer 200. Further, illumination equipment illuminates surface 262 of semiconductor wafer 200 so as to assure a sufficient concentration of holes for the anodic etching process. The size and shape of the high aspect ratio holes through semiconductor wafer 200 depends on, for example, the anodization parameters such as HF concentration, current density, and light illumination. An anodic etching process is described in V. Lehmann, *The Physics of*

Macropore Formation in Low Doped n-Type Silicon, J. Electrochem. Soc., Vol. 140, No. 10, pp. 2836-2843, Oct. 1993, which is incorporated herein by reference.

As shown in Figures 5 and 6, reflective layer 254 is formed on inner surface 252 of high aspect ratio holes 250. In one embodiment, reflective layer 254 comprises a metallic mirror that is deposited with a self-limiting deposition process. This produces a reflective surface for optical waveguide 256 that is substantially uniform. Waveguide 256 also has a center void 258 that is essentially filled with air.

A two-step, selective process is used, for example, to deposit tungsten as a portion of reflective layer 254. This is a low-pressure chemical vapor deposition (LPCVD) process. In this process, atoms in semiconductor wafer 200, e.g., silicon, are replaced by tungsten atoms in a reaction gas of WF_6. This is referred to as a "silicon reduction process." The limiting thickness of this process is approximately 5 to 10 nanometers. This thickness may not be sufficient for reflective layer 254. Thus, a second reduction process can be used to complete the deposition of tungsten. This second reduction step uses silane or polysilane and is thus referred to as a "silane reduction." The silane reduction process also uses WF_6. In this process, the deposition rate is highly dependent on the temperature and the reaction gas flow rate. For example, at 300° Celsius, tungsten deposits at a rate as high as 1 micron per minute using WF_6 flow rate of 4 standard cubic centimeters per minute in a cold-wall chemical vapor deposition (CVD) reactor.

When tungsten is used for reflective layer 254, a thin film of a material with a higher reflectivity is deposited on the tungsten material. For example, an aluminum film can be deposited at low temperature, e.g., in the range from 180° to 250° Celsius. Dimethylaluminum hydride is often used as the precursor when depositing aluminum because of its thermal stability and high vapor pressure. Further, the deposition of aluminum can be carried out with hydrogen as a carrier gas with wafer 200 maintained at a temperature of approximately 250° Celsius and a pressure of approximately 5 Torr. The typical deposition rate for this process is less than 100 nanometers per minute. It is noted that the aluminum could be deposited on a silicide as well. Aluminum can be

deposited on a silicide at a much lower temperature, e.g., 100° Celsius, with a very high deposition rate using dimethylethylaminealane (DMEAA). Deposition rates of 500 nanometers per minute have been reported using this technique at 150° Celsius with no carrier gas, and approximately 70 nanometers per minute at 100° Celsius.

Conclusion

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, the diameter of the opening in the optical waveguides can be adjusted as needed for a specific application. Further, process parameters can be varied so as to create high aspect ratio holes with sufficient diameter and reflective layers of sufficient thickness for a particular application. Other appropriate materials and processes can be used to form the reflective layer of the optical waveguides. Further, it is noted that the waveguides can be used to transmit signals in either direction through a semiconductor wafer. Further, electronic systems can include more than two semiconductor wafers with sufficient optical waveguides formed through the semiconductor wafers to allow signals to be communicated between the integrated circuits of the various semiconductor wafers.

Advantageously, using optical waveguides according to the teachings of the present invention allows electronic systems to be constructed in less physical space compared to conventional electronic systems by removing the need for large printed circuit boards to interconnect various integrated circuits. This also provides the advantage of reducing the cost of packaging integrated circuits for a particular electronic system by allowing a number of circuits to be packaged together. Further, using the optical waveguides assures the electrical integrity of interconnections between integrated circuits by reducing the physical length of electrical interconnections between

devices. This reduces concerns with signal loss or dissipation and interference with and by other integrated circuitry devices.

What is claimed is:

1. A method for interconnecting first and second integrated circuits, wherein the first integrated circuit is formed on a working surface of a first semiconductor substrate, the method comprising:

forming at least one high aspect ratio hole through the first semiconductor substrate;

lining the high aspect ratio hole with a material having a high reflectivity for light to form an optical waveguide; and

coupling the first integrated circuit to the second integrated circuit through the optical waveguide.

2. The method of claim 1, and further comprising forming the second integrated circuit on a second surface, opposite the working surface of the first semiconductor substrate.

3. The method of claim 1, and further comprising:

forming the second integrated circuit in a working surface of a second semiconductor substrate; and

bonding the first and second semiconductor substrates together such that the first and second integrated circuits are coupled together through the optical waveguide in the first semiconductor substrate.

4. The method of claim 3, wherein bonding the first and second semiconductor substrates together comprises bonding surfaces of the first and second semiconductor substrates that are opposite the working surfaces of the first and second semiconductor substrates.

5. The method of claim 3, wherein bonding the first and second semiconductor substrates together comprises bonding a working surface of the second semiconductor substrate with a surface of the first semiconductor substrate that is opposite the working surface of the first semiconductor substrate.

6. The method of claim 1, wherein forming at least one high aspect ratio hole comprises:

forming etch pits at selected locations in the first surface of the semiconductor substrate; and

performing an anodic etch of the first semiconductor substrate such that high aspect ratio holes are formed through the first semiconductor substrate at the location of the etch pits.

7. The method of claim 1, wherein coupling the first integrated circuit to the second integrated circuit comprises forming optical transmitters and receivers on opposite ends of the optical waveguide so as to transmit signals between the first and second integrated circuits.

8. The method of claim 7, wherein forming an optical transmitter comprises forming a gallium arsenide optical transmitter that is bonded to a surface of the first semiconductor substrate and forming an optical receiver comprises forming a silicon photodiode detector at an opposite end of the optical waveguide.

9. The method of claim 1, wherein lining the high aspect ratio hole comprises lining the high aspect ratio hole with a layer of tungsten and a layer of aluminum.

10. The method of claim 9, wherein the tungsten layer is formed using a silicon reduction process and a silane reduction process.

11. The method of claim 1, wherein lining the high aspect ratio hole comprises forming a layer of aluminum material.

12. The method of claim 11, wherein forming the layer of aluminum material comprises forming a layer of aluminum material with a thickness of approximately 300 angstroms.

13. The method of claim 1, wherein lining the high aspect ratio holes comprises leaving an opening extending through the semiconductor substrate with a cross-sectional diameter of at least three times the cut-off diameter.

14. An electronic system, comprising:

at least one semiconductor wafer;

a number of integrated circuits with at least one integrated circuit formed on the at least one semiconductor wafer;

the at least one semiconductor wafer including at least one optical waveguide formed in a high aspect ratio hole that extends through the thickness of the at least one semiconductor wafer; and

at least one optical transmitter and at least one optical receiver associated with the at least one optical waveguide that transmit optical signals between selected integrated circuits of the electronic system.

15. The electronic system of claim 14, wherein the number of integrated circuits includes a microprocessor and a memory device.

16. The electronic system of claim 14, wherein the at least one optical waveguide comprises at least one optical waveguide that is formed by an anodic etch that creates at least one high aspect ratio hole through the semiconductor wafer that is lined with a highly reflective material.

17. The electronic system of claim 14, wherein the at least one optical waveguide includes a metallic mirror that lines an inner surface of the high aspect ratio hole.

18. The electronic system of claim 17, wherein the metallic mirror includes a layer of tungsten formed on the inner surface of the high aspect ratio hole and a layer of aluminum formed outwardly from the layer of tungsten.

19. The electronic system of claim 17, wherein the tungsten layer is formed using a silicon reduction process and a silane reduction process.

20. The electronic system of claim 14, wherein the at least one optical waveguide has a cross-sectional diameter of at least three times the cut-off diameter.

21. The electronic system of claim 14, wherein the at least one optical waveguide comprises a layer of aluminum material that lines the high aspect ratio holes.

22. The electronic system of claim 21, wherein the layer of aluminum material has a thickness of approximately 300 angstroms.

23. An integrated circuit, comprising:

a functional circuit formed on a wafer;

a number of optical waveguides formed in high aspect ratio holes that extend through the wafer; and

wherein the optical waveguides include a highly reflective material that is deposited so as to line an inner surface of the high aspect ratio holes.

24. The integrated circuit of claim 23, wherein the number of optical waveguides comprises optical waveguides that are formed by an anodic etch that creates high aspect

ratio holes through the semiconductor wafer that are lined with a highly reflective material.

25. The integrated circuit of claim 23, wherein each optical waveguide includes a metallic mirror that lines an inner surface of the high aspect ratio hole.

26. The integrated circuit of claim 25, wherein the metallic mirror includes a layer of tungsten formed on the inner surface of the high aspect ratio hole and a layer of aluminum formed outwardly from the layer of tungsten.

27. The integrated circuit of claim 26, wherein the tungsten layer is formed using a silicon reduction process and a silane reduction process.

28. The integrated circuit of claim 23, wherein the optical waveguides have a cross-sectional diameter of at least three times the cut-off diameter.

29. The integrated circuit of claim 23, wherein the optical waveguides comprise a layer of aluminum material that lines the high aspect ratio holes.

30. The integrated circuit of claim 29, wherein the layer of aluminum material has a thickness of approximately 300 angstroms.

31. A method for forming an integrated circuit in a semiconductor wafer with an optical waveguide that extends through the semiconductor wafer, the method comprising:

forming a functional circuit in a first surface of the semiconductor wafer;

forming a number of etch pits in the first surface of the semiconductor wafer at selected locations in the functional circuit;

performing an anodic etch of the semiconductor wafer such that high aspect ratio holes are formed through the semiconductor wafer from the first surface to a second, opposite surface;

forming a highly reflective layer of material on an inner surface of the high aspect ratio holes such that the holes have an opening extending through the semiconductor wafer with a diameter that is at least three times the cut-off diameter; and

selectively coupling the optical fiber to the functional circuit.

32. The method of claim 31, wherein forming a highly reflective layer includes forming a metallic mirror that lines an inner surface of the high aspect ratio hole.

33. The method of claim 32, wherein forming the metallic mirror includes forming a layer of tungsten on the inner surface of the high aspect ratio hole and forming a layer of aluminum outwardly from the layer of tungsten.

34. The method of claim 33, wherein forming the tungsten layer includes using a silicon reduction process and a silane reduction process.

35. The method of claim 31, wherein forming the highly reflective layer includes lining the high aspect ratio holes with a layer of aluminum material.

36. The method of claim 35, wherein lining the high aspect ratio holes with the layer of aluminum material includes lining the high aspect ratio holes with a layer of aluminum that has a thickness of approximately 300 angstroms.

37. A method for forming an optical waveguide through a semiconductor substrate, the method comprising:

forming at least one high aspect ratio hole through the semiconductor substrate that passes through the semiconductor substrate from a first working surface to a surface opposite the first working surface; and

lining the high aspect ratio hole with a material having a high reflectivity for light.

38. The method of claim 37, wherein forming the at least one high aspect ratio hole comprises etching high aspect ratio holes in the semiconductor substrate using an anodic etch.

39. The method of claim 38, and further comprising forming etch pits in the working surface of the semiconductor substrate prior to the anodic etch such that the at least one high aspect ratio hole is formed at the location of the etch pits.

40. The method of claim 37, wherein lining the high aspect ratio hole comprises lining the high aspect ratio hole with a layer of tungsten and a layer of aluminum.

41. The method of claim 40, wherein the tungsten layer is formed using a silicon reduction process and a silane reduction process.

42. The method of claim 37, wherein lining the high aspect ratio hole comprises forming a layer of aluminum material.

43. The method of claim 42, wherein forming the layer of aluminum material comprises forming a layer of aluminum material with a thickness of approximately 300 angstroms.

44. The method of claim 37, wherein lining the high aspect ratio holes comprises leaving an opening extending through the semiconductor substrate with a cross-sectional diameter of at least three times the cut-off diameter.

Abstract of the Disclosure

An integrated circuit with a number of optical waveguides that are formed in high aspect ratio holes. The high aspect ratio holes extend through a semiconductor wafer. The optical waveguides include a highly reflective material that is deposited so as to line an inner surface of the high aspect ratio holes which may be filled with air or a material with an index of refraction that is greater than 1. These metal confined waveguides are used to transmit signals between functional circuits on the semiconductor wafer and functional circuits on the back of the wafer or beneath the wafer.

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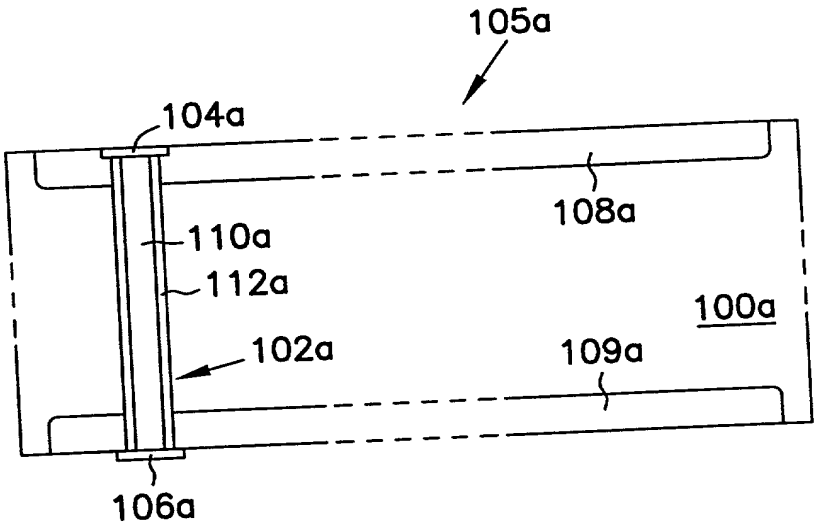
Printed Name Shawn Hise

Signature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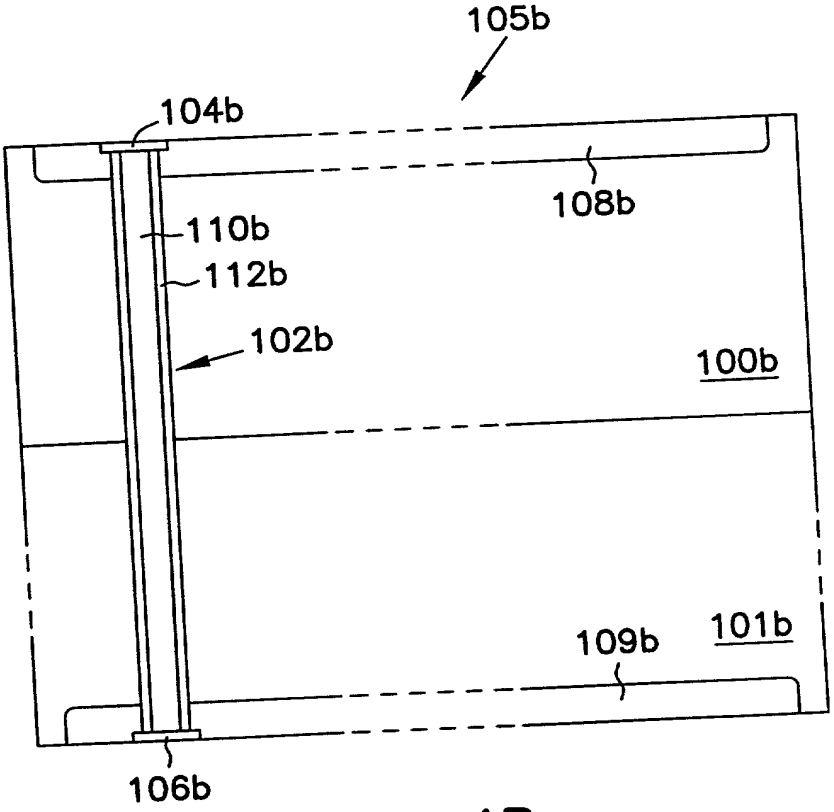
104a
108a
110a
112a
100a
102a
109a
106a

FIG. 1A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108b
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109b
101b
106b

FIG. 1B

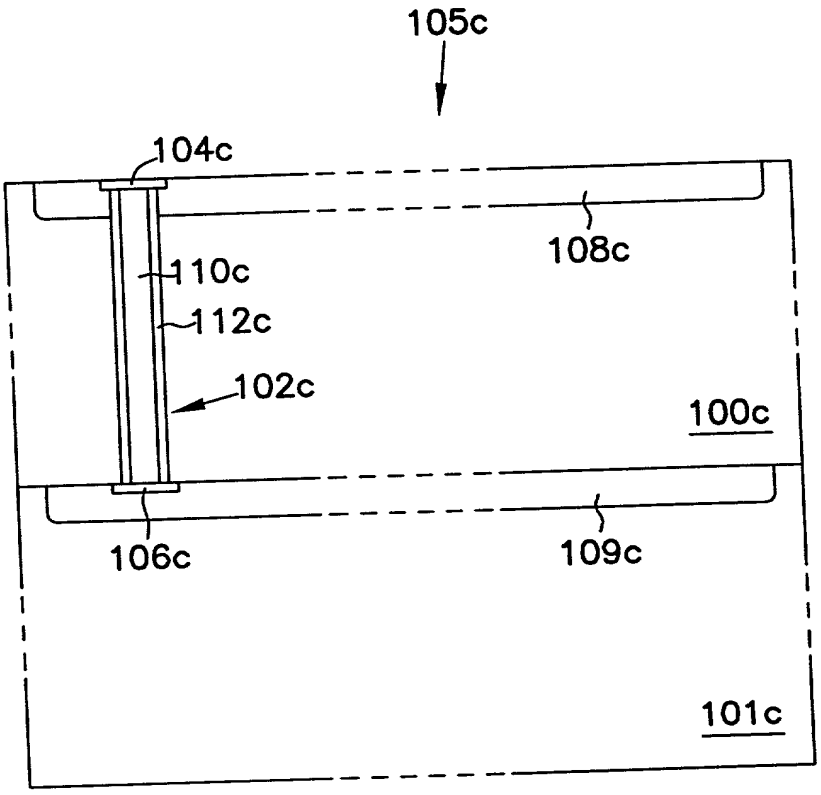

FIG. 1C

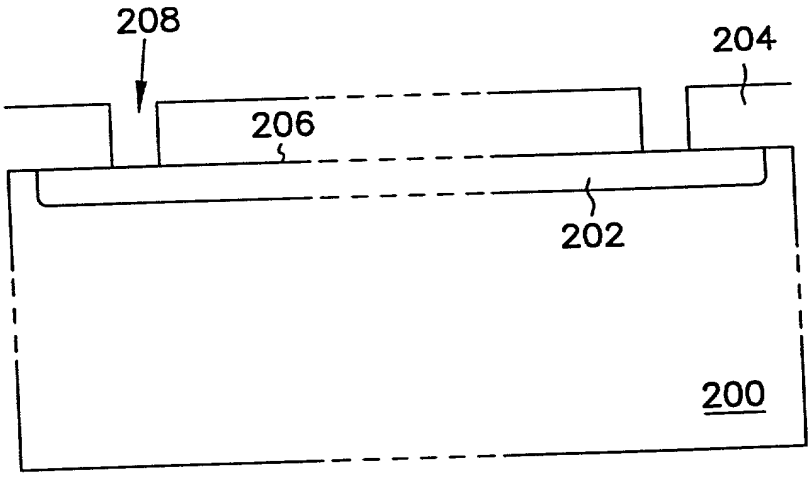

FIG. 2

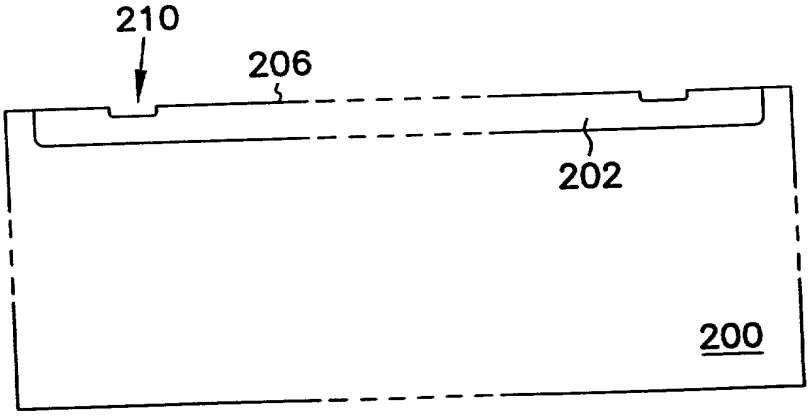

FIG. 3

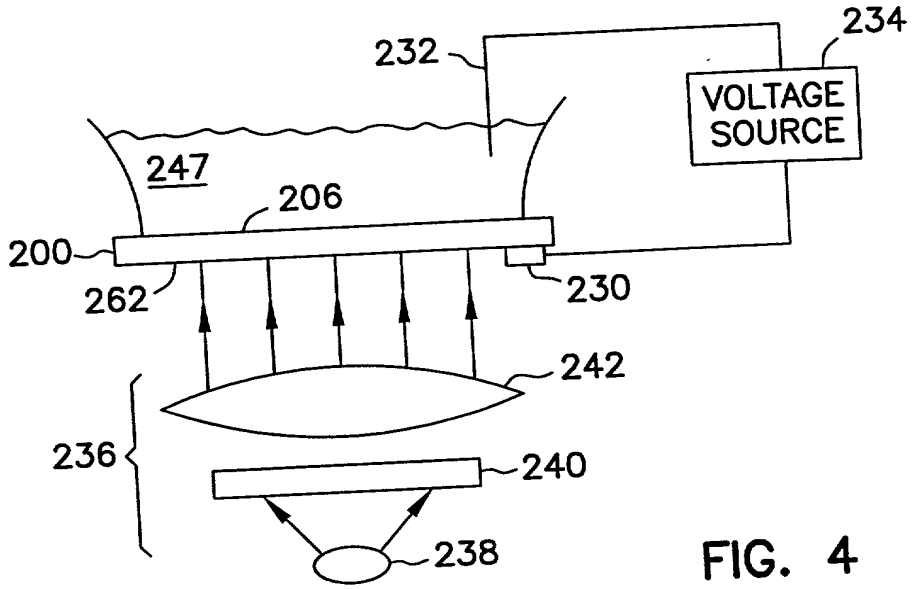
232
234
VOLTAGE SOURCE
247
206
200
262
230
242
236
240
238

FIG. 4

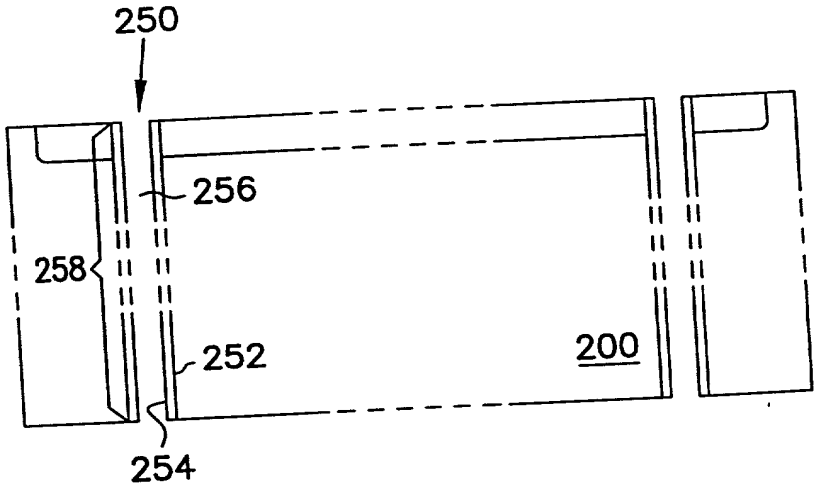
250
256
258
252
200
254

FIG. 5

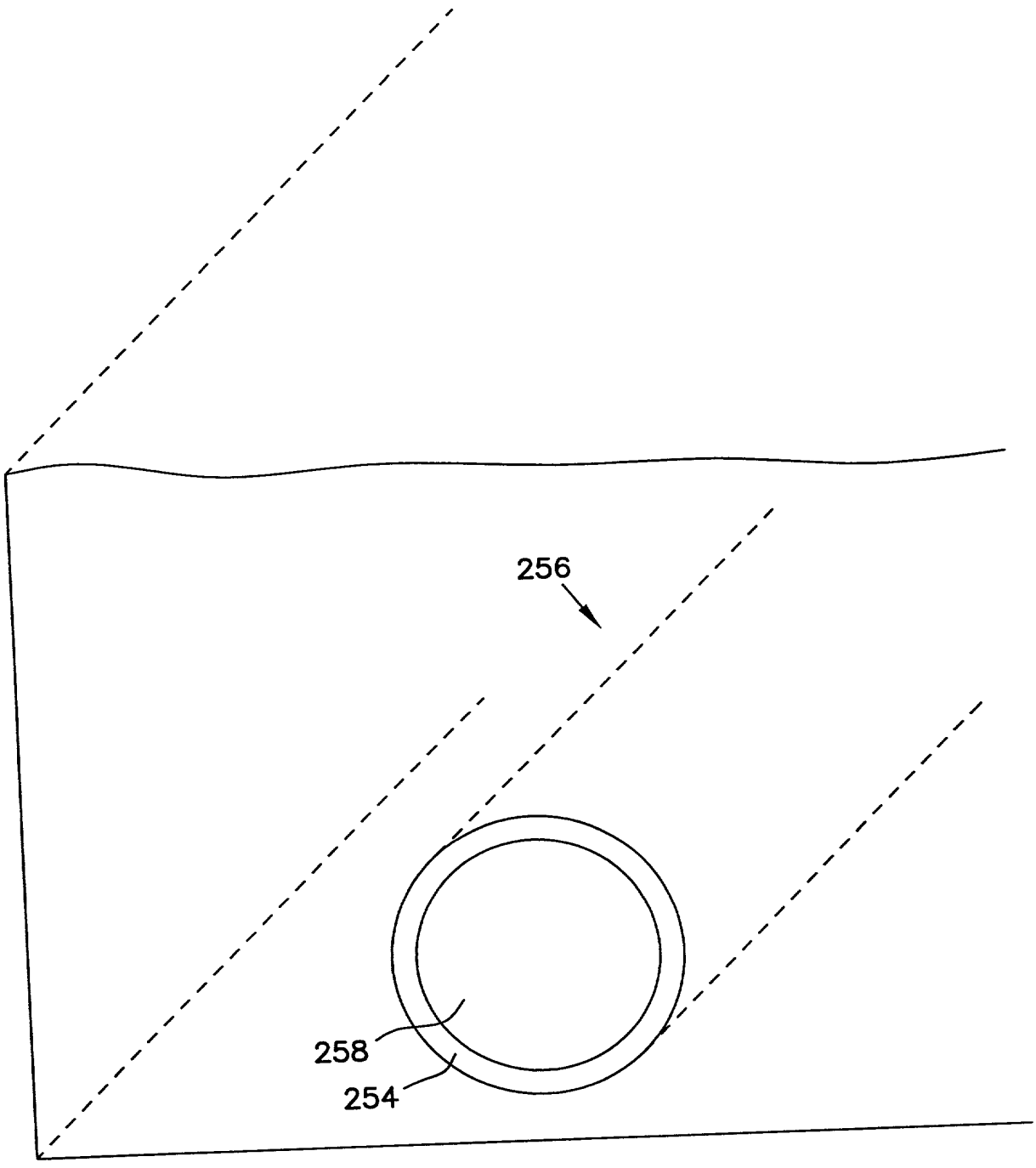

FIG. 6

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first an joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

INTEGRATED CIRCUITS USING OPTICAL WAVEGUIDE INTERCONNECTS FORMED THROUGH A SEMICONDUCTOR WAFER AND METHODS FOR FORMING SAME .

The specification of which was filed on February 26, 1998 as application serial no. 09/031,961.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such applications have been filed.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such applications have been filed.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such applications have been filed.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Joseph E. Geusic**
Citizenship: **United States of America** Residence: **Berkeley Heights, NJ**
Post Office Address: 261 Lorraine Drive
Berkeley Heights, NJ 07922

Signature: Joseph E. Geusic Date: 4/22/98
Joseph E. Geusic

Full Name of joint inventor number 2 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: _____ Date: _____
Kie Y. Ahn

Full Name of joint inventor number 3 : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: _____
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Post Office Address: 261 Lorraine Drive
Berkeley Heights, NJ 07922

Signature: _____ Date: _____
Joseph E. Geusic

Full Name of joint inventor number 2 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
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Chappaqua, NY 10514

Signature: Kie Y. Ahn Date: 4-14-98
Kie Y. Ahn

Full Name of joint inventor number 3 : **Leonard Forbes**
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Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: _____
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Citizenship: **United States of America** Residence: **Berkeley Heights, NJ**
Post Office Address: 261 Lorraine Drive
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Signature: _____ Date: _____
Joseph E. Geusic

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Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: _____ Date: _____
Kie Y. Ahn

Full Name of joint inventor number 3 : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: 11 APR 98
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

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§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Joseph E. Geusic et al.	Examiner: Unknown	
Serial No.:	09/031,961	Group Art Unit: Unknown	
Filed:	February 26, 1998	Docket: 303.382US1	
Title:	INTEGRATED CIRCUITS USING OPTICAL WAVEGUIDE INTERCONNECTS FORMED THROUGH A SEMICONDUCTOR WAFER AND METHODS FOR FORMING SAME		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Anglin, J. Michael	Reg. No. 24,916	Forrest, Bradley A.	Reg. No. 30,837	Lundberg, Steven W.	Reg. No. 30,568
Arora, Suneel	Reg. No. P-42,267	Hale, Jeffrey D.	Reg. No. 40,012	Madrid, Andres N.	Reg. No. 40,710
Bernkopf, Paul A.	Reg. No. P-41,615	Harris, Robert J.	Reg. No. 37,346	McCrackin, Ann M.	Reg. No. P-42,858
Bianchi, Timothy E.	Reg. No. 39,610	Hofmann, Rudolph P., Jr.	Reg. No. 38,187	Provence, David L.	Reg. No. P-43,022
Billion, Richard E.	Reg. No. 32,836	Holloway, Sheryl S.	Reg. No. 37,850	Schwegman, Micheal L.	Reg. No. 25,816
Brennan, Thomas F.	Reg. No. 35,075	Huebsch, Joseph C.	Reg. No. P-42,673	Simboli, Paul B.	Reg. No. 38,616
Brooks, Edward J., III	Reg. No. 40,925	Klima-Silberg, Catherine I.	Reg. No. 40,052	Slifer, Russell D.	Reg. No. 39,838
Clark, Barbara J.	Reg. No. 38,107	Kluth, Daniel J.	Reg. No. 32,146	Taylor, Michael W.	Reg. No. P-43,182
Drake, Eduardo E.	Reg. No. 40,594	Leffert, Thomas W.	Reg. No. 40,697	Terry, Kathleen R.	Reg. No. 31,884
Dryja, Michael A.	Reg. No. 39,662	Lemaire, Charles A.	Reg. No. 36,198	Viksnins, Ann S.	Reg. No. 37,748
Embretson, Janet E.	Reg. No. 39,665	Litman, Mark A.	Reg. No. 26,390	Woessner, Warren D.	Reg. No. 30,440
Fogg, David N.	Reg. No. 35,138				

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

Schwegman, Lundberg, Woessner & Kluth, P.A.
Attn: David N. Fogg
P.O. Box 2938
Minneapolis, MN 55402

Telephone: (612) 373-6920
Facsimile: (612) 339-3061

Dated: May 22, 1998

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel